REMARKS

Favorable reconsideration of the present patent application is respectfully requested in view of the following remarks. No claims are added, canceled or substantively amended in this paper. Claims 10 and 15 are amended to address minor informalities, that is, typographical errors. Claims 1-16 remain pending in the application.

In the Office Action dated April 20, 2005, claims 16 is rejected under 35 U.S.C. §112, first paragraph as purportedly failing to comply with the enablement requirement. Claims 1-3, 5-6, 8-9, 11 and 13 are rejected under 35 U.S.C. §103(a) in view of U.S. Patent 5,592,508 (Cooper) and further in view of U.S. Patent 6,215,737 (Thagard). Claims 12 and 16 are rejected under 35 U.S.C. §103(a) in view of U.S. Patent 5,774,567 (Heyl) and further in view of the Thagard patent. Claims 4 and 10 are rejected under 35 U.S.C. §103(a) in view of the Cooper patent and further in view of the Thagard patent and yet further in view of U.S. Patent 6,052,471 (Van Ryzin). Claim 7 is rejected under 35 U.S.C. §103(a) in view of the Cooper patent and further in view of the Thagard patent and yet further in view of the Heyl patent. Claims 14 and 15 are rejected under 35 U.S.C. §103(a) in view of the Cooper patent and further in view of the Thagard patent and yet further in view of U.S. Patent 5,153,592 (Fairchild). It is respectfully submitted that these rejections should be withdrawn for at least the following reasons.

35 U.S.C. §112, First Paragraph Rejection

Claim 16 was rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement. The enablement requirement is separate and distinct from the written description requirement. The enablement requirement refers to the requirement of 35 U.S.C. §112, first paragraph that the specification describe how to make and how to use the

invention. The Manual of Patent Examining Procedure (MPEP) sets forth the test for determining whether an invention is enabled by the specification:

> The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation.[1]

With regard to the Office's contention that claim 16 is not enabled, it is noted that nearly all computers have internal speakers which receive analog signals converted from a D/A converter. it is believed that all (or nearly all) of the personal computers at the U.S. Patent and Trademark Office include such speakers. Certainly it did not take undue experimentation to include speakers with these computers. Consequently, it is respectfully submitted that the computer system of claim 16 comprising "a computer speaker configured to receive analog signals converted from the digital audio signals by the selected digital-to-analog converter," meets the enablement requirement of §112, first paragraph.

Moreover, it is respectfully submitted that the specification meets the § 112, first paragraph written description requirement, as well. The specification explains that "[t]hese analog signals may then be played through a speaker internal to the computer, or amplified and played through external speakers."[2]

Accordingly, withdrawal of the rejection of claim 16 under §112, first paragraph, is respectfully requested.

§103 Rejection in view of Cooper / Thagard

Claims 1-3, 5-6, 8-9, 11 and 13 are finally rejected under §103 in view of the Cooper / Thagard hypothetical combination. It is believed that this rejection cannot be maintained for at least the following reasons.

[1] MPEP 2164.01, page 2100-185.

No teaching of a Computer System

Independent claims 1 and 2 recite "a personal computer system," and independent method claims 9, 11 and 13 recite a "method of routing digital audio ... in a personal computer." The Cooper and Thagard patents relied upon in the Office Action do not teach a personal computer system comprising the elements of the claimed invention, and do not even appear to pertain to personal computer systems. As pointed out in the previous Amendment of June 30, 2005, the various patents cited in the Office Action may have a computer mentioned as a component of the system.[3] However, the systems described in the cited patents are not themselves personal computer systems. Hence, the Cooper and Thagard patents cited in the Office Action do not teach or suggest a personal computer or method of routing digital audio in a personal computer.

The pending final Office Action of September 19, 2005 points to passages in columns 3-5 of Cooper and contends that "Cooper teaches the method of routing digital audio to D-A converter and a computer." (Citations omitted). This contention is respectfully traversed. The cited passages of the Cooper patent are attached to this paper as Appendix A. A further, careful review of all the patents cited in the pending rejection, and in particular, the Cooper patent, again did not uncover any teaching of a computer with the elements alleged in the Office Action. It is not understood where—either in the cited passages or anywhere else in the patents relied upon in the pending rejection—that there is a teaching of "a personal computer system" or a "method of routing digital audio ... in a personal computer."

In the event the final rejection is not withdrawn, it is respectfully requested that the next paper from the Office point to any teaching in the relied-upon patents of a "a personal computer system" comprising the elements recited in 1, 2 and 12 and a "method of routing

[2] Specification, page 1, lines 11-12.

digital audio ... in a personal computer" comprising the elements recited in claims 9, 11 and 13.

Further, in the event the final rejection is not withdrawn, it is respectfully requested that the next paper from the Office point to any teaching in the relied-upon patents of a "a personal computer system" comprising the elements recited in 1, 2 and 12 and a "method of routing digital audio ... in a personal computer" comprising the elements recited claims 9, 11 and 13.

Other Elements Missing from Cooper and Thagard

It is believed that there are other features of the claims that are not taught or suggested by the patents cited in the rejection. The previous Amendment filed on June 30, 2005, included remarks pointing out that the Cooper patent lacked various features of the claims, for example, Cooper does not teach to route audio signals based on differences in quality. It is appreciated that the grounds of rejection in the final Office Action have been changed to now acknowledge that Cooper does not teach the routing of audio signals based on differences in quality. However, the pending final Office Action now contends that the Thagard patent teaches features which overcome this deficiency of Cooper. This contention is traversed.

The device described in the Thagard patent records a multi-channel audio source and plays it back using different sampling rates for the various channels of the audio source. Even if one equates sampling rate to quality, the different sampling rates discussed in Thagard are used in the various channels of *a single signal source.* The Thagard patent does not teach different sampling rates—or any other measure of quality—for different audio sources. The Thagard patent does not teach or suggest the various features of the claims missing from the Cooper patent. For example, various claims now pending in the application recite signals from multiple

[3] Cooper, For example, N-bit channel #9 shown in Fig. 2; col. 3, lines 23-30.

sources being routed based upon the desired quality of the converter, a feature which is not taught in either Cooper or Thagard:

- Claim 1 recites a controller which routes digital audio signals "from multiple sources ... to a selected digital-to-analog converter based on a desired converter quality."
- Claim 9 recites "routing digital audio data [from one of a plurality of audio sources] based on desired converter quality."
- Claim 11 recites "routing [from one of a plurality of audio sources] in an order determined by the assigned data priority."
- Claim 13 recites "routing digital audio signals from standard digital audio sources to a standard quality digital-to-analog converter" and "routing digital audio signals from high-quality audio sources to a high-quality digital-to-analog converter." (Emphasis added).

The Thagard device samples various channels of a single audio source at different sampling rates. The Thagard patent does not concern signals from multiple audio sources, or a desired converter quality for the signals from multiple audio sources. Consequently, Thagard does not overcome the deficiencies of the Cooper patent.

It is noteworthy that in one part of the Office Action the Office rejects claims 14 and 15, adopting the position that "Cooper and Thagard do not clearly teach that each of the plurality of audio digital-to-analog converters has an indication of quality."[4] Yet in the rejection of claims 1 and 9 (from which claims 14 and 15 respectively depend) the Office apparently adopts the position that Thagard teaches to "route the digital audio signals to a selected digital-to-analog converter based on a desired converter quality," as recited in claim 1, and the similar feature of claim 9. These two positions adopted by the Office seem to be at odds with each other. **In the event the pending final rejection is maintained, it is respectfully requested that the next paper explain how the Thagard device can route digital audio signals to a selected digital-to-analog converter based on a desired converter quality (claim 1), and yet the Thagard patent does not clearly teach that each of the plurality of audio digital-to-analog converters has an indication of quality (as admitted in the rejection of claims 14-15).**

Accordingly, the Cooper patent and the Thagard patent, either taken singly or as a hypothetical combination, do not teach or suggest the features of claims 1-3, 5-6, 8-9, 11 and 13. It is respectfully requested that the §103 rejection in view of Cooper and further in view of Thagard be withdrawn.

§103 Rejection in view of Heyl / Thagard

Claims 12 and 16 are finally rejected under §103(a) in view of the Heyl / Thagard hypothetical combination. It is believed that this rejection cannot be maintained for at least the following reasons.

No teaching of a Computer System

Independent claim 12 recites "a personal computer system." The Heyl and Thagard patents relied upon in the Office Action do not teach a personal computer system comprising the elements of claims 12 and 16. The Thagard is discussed above. The Heyl patent is drawn to an audio codec. An audio codec—as discussed in the Heyl patent—is *not* a personal computer system. However, a computer system may contain an audio codec. In fact, the very first sentence in column 1 of the Heyl patent expressly states that the "present invention (of the Heyl patent) relates to codecs, and more particularly, to audio codecs suitable for supporting sophisticated multimedia functions within personal computers." Hence, the Heyl and Thagard patents cited in the Office Action do not teach or suggest a personal computer system, for example, with the features recited in claim 12 (e.g., with a processor).

Other Elements Missing from Heyl and Thagard

The Office Action acknowledges that "Heyl does not clearly teach to route the digital audio signals to a selected digital-to-analog converter based on desired converter quality." As

[4] Office Action of September 19, 2005, at page 8, paragraph 9.

discussed above, the Thagard patent does not teach this feature either. The Thagard device uses different sampling rates for the various channels of a single multi-channel audio source. Thagard does not receive multiple audio sources, and is not concerned with a desired converter quality for the signals from multiple audio sources. Consequently, Thagard does not overcome the deficiencies of the Heyl patent.

Accordingly, the Heyl patent and the Thagard patent, either taken singly or as a hypothetical combination, do not teach or suggest the features of claims 12 and 16. It is respectfully requested that the §103 rejection in view of Heyl and further in view of Thagard be withdrawn.

§103 Rejections of the Dependent Claims

Claims 4 and 10 are rejected in view of the Cooper / Thagard / Van Ryzin hypothetical combination. Claim 7 is rejected in view of the Cooper / Thagard / Heyl hypothetical combination. Claims 14-15 are rejected in view of the Cooper / Thagard / Fairchild hypothetical combination.

The Van Ryzin patent is the third patent cited in the three-way §103 rejection of claims 4 and 10. The Van Ryzin patent involves receiver control circuitry which automatically detects the various signal sources available and then selects a signal for the input to the receiver *if it has been assigned a priority*. For instance, if a user is listening to a CD player through his stereo receiver system and turns on the TV, the receiver would detect the TV input and switch over to the TV if it has a higher priority than the CD player. Although Van Ryzin teaches assigning a priority to various input sources, Van Ryzin does not teach anything about selecting a D/A converter on the basis of desired converter quality for the signals from multiple audio sources. Therefore, it is respectfully submitted that the system described in the Van Ryzin patent does not overcome the aforementioned deficiencies of the hypothetical Cooper / Thagard combination.

Accordingly, it is respectfully requested that the §103 rejection of claims 4 and 10 in view of the Cooper / Thagard / Van Ryzin hypothetical combination be withdrawn.

The Heyl patent is the third patent cited in the three-way §103 rejection of claim 7. The Heyl patent, discussed above in regard to the rejection of claims 12 and 16, does not overcome the aforementioned deficiencies of the hypothetical Cooper / Thagard combination. Accordingly, it is respectfully requested that the §103 rejection of claim 7 in view of the Cooper / Thagard / Heyl hypothetical combination be withdrawn.

The Fairchild patent is the third patent cited in the three-way §103 rejection of claims 14-15. The Fairchild patent involves an improved D/A conversion circuit. The Fairchild patent does not teach or suggest a personal computer or method of routing digital audio in a personal computer. The Fairchild patent does not disclose signals from multiple audio sources, or a desired converter quality for the signals from multiple audio sources. Therefore, the Fairchild patent does not overcome the deficiencies of the Cooper / Thagard hypothetical combination. Accordingly, it is respectfully requested that the §103 rejection of claims 14-15 in view of the Cooper / Thagard / Fairchild hypothetical combination be withdrawn.

Deposit Account Authorization / Provisional Time Extension Petition

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 50-0439 and please credit any excess fees to such deposit account.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. However, should there remain any unresolved issues, the Examiner is kindly invited to contact applicant's representative, Scott Richardson, at telephone number 1.703.739.0573 so that such issues may be resolved as expeditiously as possible.

Respectfully submitted,

Scott Charles Richardson
Registration No. 43,436

128 North Pitt Street, 2nd Floor
Alexandria,VA 22314
1.703.740.8322

Date: November 15, 2005

Attachments:
Appendix A (U.S. Patent 5,592,508 (Cooper) columns 3-6)

Appendix A

analog and digital and signals, it should be kept in mind that the functions described may well be implemented with optical or electronic embodiments or a combination of both, there being optical equivalents for most electronic signals, for example digital optical video signal and digital electronic video signals, electronic clock generators and optical clock generators, etc. While the optical signal processing art sometimes utilizes different terminology, it will be understood that the electronic art terminology utilized herein is intended to encompass equivalent functions, devices and operations in the optical art.

FIG. 2 shows input terminal 7, analog to digital convertor 13 made up of N-bit serial coder 8 and operative to provide a serial N-Bit digital output signal for both analog and digital input signals, A-D 13 further including a high frequency clock generator 12, N-Bit serial channel 9, which may be of synchronous or asynchronous form, and D-A 10 to provide a digital or analog output signal at output terminal 11, D-A 10 including an N-Bit digital serial decoder to provide an analog signal output when an analog signal is input or a digital signal output when a digital signal is input.

It may be understood that a feature of the present invention is to facilitate the transport, coupling and use of various optical and electronic signals. The channel 9 represents many such types of transport, coupling and use, and is not specific to any particular utilization of the digital signal. It should also be noted that other methods of transmission may be utilized in channel 9, including modulated radio frequency energy and optical energy such as fiber optics, storage, such as computer or other type floppy or hard disk or Optical disk or matrix. It will be apparent to one skilled in the art from the teachings herein a method and apparatus is shown for conveniently and efficiently passing or converting input signals of a variety of types into a convenient digital form. Once the input signal is available from 13 in digital form, that digital signal may be carried or utilized in any number of fashions as are well known to one skilled in the art. It should also be noted that the A-D section 13 is useful by itself, that is without any immediate reconversion of the digital signal back to its original form, for example it may be desired to simply store the digital signal from 13 for archival or storage purposes.

For the function of generating a clock, which is phase locked to a digital bit stream as provided by 12, it is preferred that the phase locking circuit be a GS9005 supplied by Gennum Corporation of Burlington, Ontario, Canada. The GS9005 receives a digital bit stream and provides a bit clock via internal PLL. In addition, if it is desired to equalize the digital bit stream due to long cable runs, a Gennum GS9004 is well suited to this application. For analog signals, it is sufficient that the clock signal be asynchronous but stable, which the Gennum part will provide if the input signal is removed. Alternatively, the functions of 12 may be implemented in a standard cell ASIC. Gallium Arsenide technology is preferred for such ASIC and the ALSI Standard cells from TriQuent Semiconductor of Beaverton, Oregon is preferred for these circuits.

It should be noted that while applicant has referred to element 13 as an A-D convertor and element 10 as a D-A convertor, that these elements actually perform differently from the same named elements which are commonly known in the art. Applicant applies a different and much broader meaning to these names, which meaning will become apparent from the teachings herein. For a broad description of these elements, one skilled in the art should understand that both digital and analog signals may be input to A-D signal 13 and both digital and analog signals may be output from D-A 10. It is important to note that one of the features of the present invention is that a given input signal may be changed to or preserved as a high frequency serial digital bit stream, this bit stream being operated on in a relatively inexpensive manner and then output in a desired form. This operation is novel including the feature that by using a single serial bit stream to convey the input signal, no matter what the input signal form, format or bandwidth, the processing, transmission and routing of the serial bit stream is the same for all input signal types.

Normally, it is preferred that the format of the output signal match the format of the input signal, for example analog in/analog out, digital in/digital out, a given format in/the same format out. It will be understood from the teachings herein, that there is nothing preventing one skilled in the art from combining functions and adding circuitry to allow mixing and conversion such that the input and output signals may very well not be the same. Although the invention is described in its preferred embodiment as having the same type and format signal input and output, it will be understood that this teaching actually pertains to having a known relationship between the input and output such that for a given input a given output may be obtained, said relationship being controllable as desired.

FIG. 3 is a block diagram of a second embodiment of the invention showing input terminal 7, analog to digital convertor 13 made up of N-bit serial coder 8 and operative to provide a serial N-Bit digital output signal for both analog and digital input signals, A-D 13 further including a high frequency clock generator 12 which is responsive to the input signal to either synchronize the clock thereto or determine the type of input signal and adjust Coder 8 in response thereto or both, the second embodiment having a synchronous N-Bit serial channel 9 which transmits the digitized input signal and may also transmit a clock signal from 12 to 14 and may also transmit signals to decoder 15 from coder 8 in response to the input signal or clock generator.

FIG. 3 further includes D-A 10 to provide a digital or analog output signal at output terminal 11, D-A 10 including an N-Bit digital serial decoder to provide an analog signal output when an analog signal is input or a digital signal output when a digital signal is input, with clock recovery circuit 14 responsive to either a clock related signal from 12 or to the digitized input signal from 8 to generate a recovered clock signal which is coupled to 15. The clock recovery circuit 14 is similar in function to clock generator 12 and is also preferred to be constructed of a Gennum GS9005.

FIG. 4 is a block diagram of the present invention implemented as a routing switcher configured to couple N inputs to N outputs. While the square NxN switching configuration is described, it will be understood that under the teachings herein that any switching configuration may be utilized, for example Nx1, N+Mx or other rectangular or polygonal configurations, including follow and break away configurations as are common in the art.

FIG. 4 shows N input A-D circuits 13-1 through 13-N, each responsive to an input signal 1-N and operating as previously described for element 13 of FIG. 2 or 3, a digital crosspoint array 16 configured to connect any of the digital data streams from 13-1 through 13-N to N outputs in any configuration, D-A convertors 10-1 through 10-N configured to receive the N digital data streams from the crosspoint array 16 and provide a digital output or analog output matching the particular input signal which is coupled to the D-A via 16 as appropriate. Crosspoint 16 is preferred to be

Appendix A (con't)

constructed with one or more TQ8032-M 32x32 digital cross point switches provided by TriQuent Semiconductor. FIG. 4 further includes a control circuit 17 which operates to control the switching of 16 under operator or automatic operation, control 17 further controlling the A-D circuits 13 and D-A circuits 10 to allow usage of these circuits with different types of signals, for example, digital, analog, audio and video. It is preferred that control circuit 17 be implemented with a general purpose microcontroller such as the Intel 8051 series. Inclusion of LCD display and interactive devices such as keyboards and remote keypads is quite useful for many applications.

As an example, to assist in understanding the function of the control 17, it would respond to the input signal 1 via A-D 13-1 to automatically receive information of the nature of the input signal 1, for example PAL digital video, and in turn configures. 13-1 for operation with this particular signal type, for example by adjusting the gain of conditioner 18 (described later), selecting phase locking of clock generator 12 to the digital data stream of 1. In addition, control 17 operates to configure any particular D-A, for example 10-2 to operate with the PAL digital video when the crosspoint connecting 13-1 to 10-2 is closed. In this manner, the D-As 10 can be quickly configured for optimum performance for each type of signal which is being sent to it from the crosspoint 16. It is preferred that control 17 perform other functions as well, such as preventing the coupling of inappropriate signal types to the outputs, preventing unused inputs from being coupled to outputs, allowing only certain input signals to be coupled to certain outputs, either on a continuous basis or on a time changing basis, and providing emergency alternate connection if a particular input should experience some difficulty, or if a higher priority input came available or active. For example, if a device capable of handling only analog NTSC signals were connected to a particular output, control 17 would operate to allow only analog NTSC signals to be coupled to that output. Of course, if a previously different signal on a given input were changed to an analog NTSC signal, it could then be automatically included in the list of signals available to that output in response and interaction with the A-D circuit.

The control 17 may also operate to facilitate conversion of the input signal from one type to another, for example from analog to digital, by configuring additional circuitry as required. A PAL digital signal might be converted to an NTSC analog signal for example, or an analog input signal might be output as a digital signal as needed.

It should be noted that only single dotted lines are shown connecting control 17 to A-D circuits 13 and D-A circuits 10, however, it will be understood that these lines represent multiple and bidirectional interconnections as required for a particular application, and as will be easily constructed by one skilled in the art from the teachings herein.

FIG. 5 shows a detailed block diagram of the preferred embodiment of the N-BIT digital serial coder 8 of FIGS. 2 and 3. The input signal from input terminal 7 is coupled to a signal conditioner 18 and if desired to a selector circuit 33. The conditioner 18 buffers, adjusts the gain, equalizes, DC restores and provides other processing and conditioning of the signal as necessary as is well known to one skilled in the art. Conditioner 18 may also operate to receive an optical signal and convert it to an electrical signal by use of photo transistor or photo diode circuits as is well known in the art. It is preferred that conditioner 18 utilize a Gennum GS9004 for equalization and GS9550 for receiving and buffering digital input signals, and a Gennum GB4550A and GS4981 for receiving and buffering analog signals. Conditioner 18 also provide sample and hold function in response to the clock from 12 to output a sampled and held signal 34 for use by comparator 19 as is known in the art. It will be noted that if the rate of change of the input signal over one clock is less than 1 LSB of D/A 22 that the sample and hold function may be eliminated. In addition, the conditioner 18 may operate to provide novel adjustment the gain of the signal so that the optimum signal to noise to bandwidth ratio of analog to digital conversion may be obtained in the analog to digital conversion process. Select circuit 33 operates to detect the type of signal being input, and adjust the conditioner 18 and the adaptive accumulator parameters as desired to fit the particular signal type. The select circuit 33 may also communicate with control 17 of FIG. 4, or other control circuitry as appropriate.

FIG. 5 also shows a high speed comparator 19, preferred to be an SP93802 from Plessy Semiconductor of Scotts Valley, Calif. The comparator determines if the conditioned input signal 34 from 18 is greater or less than the reference 35 from 23. If the input is greater, a digital 1 is output and if the input is less, a digital 0 is output. While it is preferred that 19 be a one bit output device, it will be recognized by one skilled in the art that other than one bit comparators may be utilized to advantage to determine both whether the input is larger or smaller than the reference, but also how much. This capability is indicated by a width O on the output of 19 and 20. The parameter of how much greater or smaller is useful to the adaptive accumulator to change step size. The output of the comparator is latched in 20 and applied to an adaptive accumulator 21. The adaptive accumulator 21 keeps track of a number of past samples, and outputs an M bit wide digital number, which is a digital estimate of the amplitude value (in PCM like format) of the next sample of input signal from 18. It will be understood that the parameters and operation of 21 may be changed in response to a controller like 17 of FIG. 4 in order to adapt 21 to a particular input signal. This digital amplitude value is converted to an analog signal by D-A convertor 22, preferred to be a TQ6140 from TriQuent. The analog signal out-of D-A 22 is filtered by 23 to remove clock energy and the resulting filtered signal is coupled as the reference to comparator 19. The filter 23 is of standard analog type as will be known to one skilled in the art, and is preferred to be supplied by Matthey Filters, available from Television Equipment Associates, Inc. of South Salem, N.Y. It will be appreciated that if there is no significant clock energy in the analog signal from 22, that filter 23 may be eliminated and the output of 22 coupled directly to 19. Digital components such as latch 20 are preferred to be implemented in standard or Gallium Arsenide 100K ECL logic such as provided by National Semiconductor of Sunnyvale, Calif.

It will be appreciated by one skilled in the art that the particular arrangement of elements shown in FIG. 5 is given by way of example, and that the elimination or rearrangement of the elements may be resorted to without departing from the spirit and scope of the invention. For example, comparators frequently contain integral latches so that latch 20 may be eliminated if 19 has an internal latch function. Elements 21 and 22 may be replaced with an analog integrator, which integrates positive and negative charges from 20 and provides an analog signal directly to 23 or 19. Other changes, which can be utilized to implement the invention in a particular form suitable for use with a particular set of input signals will be known to one of ordinary skill in the art from the teachings herein.

FIG. 6 shows a diagram of the preferred embodiment of the Adaptive Accumulator 21 of FIG. 5 which may be